Summary - DC Offset Filter

<table>
<thead>
<tr>
<th>Name</th>
<th>dc_offset_filter</th>
</tr>
</thead>
<tbody>
<tr>
<td>Worker Type</td>
<td>Application</td>
</tr>
<tr>
<td>Version</td>
<td>v1.5</td>
</tr>
<tr>
<td>Release Date</td>
<td>4/2019</td>
</tr>
<tr>
<td>Component Library</td>
<td>ocp1.assets.dsp_comps</td>
</tr>
<tr>
<td>Workers</td>
<td>dc_offset_filter.hdl</td>
</tr>
<tr>
<td>Tested Platforms</td>
<td>xsim, isim, modelsim, alt4, ml605, ZedBoard(PL), Matchstiq-Z1(PL)</td>
</tr>
</tbody>
</table>

Functionality

The DC Offset Cancellation Filter worker inputs complex signed samples, filters the DC bias from both I and Q input rails using separate 1st-order IIR filters, and outputs complex signed samples. The response time of the filter is programmable, as is the ability to bypass the filter and to update/hold the calculated DC value to be removed. For the HDL worker, a generic controls insertion of a peak detection circuit applied to the worker’s output samples.

The time constant input $TC = 128 \ast \alpha$ is limited to a signed eight-bit number, which helps to control the bit growth of the multiplier. Rearranging the equation, $\alpha = TC/128$, where a maximum value of +127 is allowed due to signed multiplication. Furthermore, $0 < \alpha < 1$ for stable operation. Larger values of $TC$ give both a faster filter response and a narrower frequency magnitude notch at zero Hertz. A typical value of $TC = 121$ ($\alpha = 0.95$) is used by default.

Worker Implementation Details

dc_offset_filter.hdl

This implementation uses a single multiplier per I/Q rail to process input data at the clock rate - i.e. this worker can handle a new input value every clock cycle. A peak detection circuit may be optionally included at build-time, which provides monitoring of the output amplitude, and may be used to influence the input gain. It is recommended to attenuate the input by one bit to prevent overflows; i.e. the input should not be driven more than half-scale to avoid overflow. This filter will produce valid output one clock cycle after each valid input.

The DC Offset Cancellation Filter worker utilizes the OCPI iqstream_protocol for both input and output ports. The iqstream_protocol defines an interface of 16-bit complex signed samples. The DATA_WIDTH_p parameter may be used to reduce the worker’s internal data width to less than 16-bits.

Figure 1: Ideal Filter Magnitude & Phase Response for $\alpha = 0.95$

Figure 2: Circuit Diagram
The BYPASS input is available to either enable (true) or bypass (false) the circuit. Note that a single bypass register is used, as shown in Figure 2 below.

**Theory**

The filter is based upon Richard G. Lyons’ “Understanding Digital Signal Processing, Third Edition” DC Removal circuit found on Page 761. The text may also be found online here: [DSP-Tricks-DC-Removal](#). Lyons’ circuit in Figure 13-62d implements the transfer function given in (13-118), which is a 1st-order IIR filter. From Lyons: “a zero resides at $z = 1$ providing infinite attenuation at DC (zero Hz) and a pole at $z = \alpha$ making the magnitude notch at DC very sharp. The closer $\alpha$ is to unity, the narrower the frequency magnitude notch centered at zero Hz.”

Adding a delay element to the output, $y$, does not change the transfer function. Moving the single delay element following the output adder to two delay elements feeding the output adder also does not change the transfer function.

**Block Diagrams**

**Top level**

![DC Offset Filter Block Diagram](#)
Source Dependencies

dc_offset_filter.hdl

- projects/assets/components/dsp_comps/dc_offset_filter/dc_offset_filter.vhd
- projects/assets/hdl/primitives/dsp_prims/dsp_prims_pkg.vhd
  projects/assets/hdl/primitives/dsp_prims/dc_offset/src/dc_offset_cancellation.vhd
- projects/assets/hdl/primitives/util_prims/util_prims_pkg.vhd
  projects/assets/hdl/primitives/util_prims/pd/src/peakDetect.vhd
## Component Spec Properties

<table>
<thead>
<tr>
<th>Name</th>
<th>Type</th>
<th>SequenceLength</th>
<th>ArrayDimensions</th>
<th>Accessibility</th>
<th>Valid Range</th>
<th>Default</th>
<th>Usage</th>
</tr>
</thead>
<tbody>
<tr>
<td>bypass</td>
<td>Bool</td>
<td>-</td>
<td>-</td>
<td>Readable, Writable</td>
<td>Standard</td>
<td>false</td>
<td>Bypass control</td>
</tr>
<tr>
<td>update</td>
<td>Bool</td>
<td>-</td>
<td>-</td>
<td>Readable, Writable</td>
<td>Standard</td>
<td>true</td>
<td>Update the calculated DC value to be removed, or hold a previously calculated value</td>
</tr>
<tr>
<td>tc</td>
<td>UChar</td>
<td>-</td>
<td>-</td>
<td>Readable, Writable</td>
<td>Standard</td>
<td>121</td>
<td>The location of the filter pole along the x-axis between 0 (the origin) and 1 (the unit circle), where $\alpha = tc/128$</td>
</tr>
<tr>
<td>messageSize</td>
<td>UShort</td>
<td>-</td>
<td>-</td>
<td>Readable, Writable</td>
<td>Standard</td>
<td>8192</td>
<td>Number of bytes in output message</td>
</tr>
</tbody>
</table>

## Worker Properties
dc_offset_filter.hdl

<table>
<thead>
<tr>
<th>Type</th>
<th>Name</th>
<th>Type</th>
<th>SequenceLength</th>
<th>ArrayDimensions</th>
<th>Accessibility</th>
<th>Valid Range</th>
<th>Default</th>
<th>Usage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Property</td>
<td>DATA_WIDTH_p</td>
<td>ULong</td>
<td>-</td>
<td>-</td>
<td>Readable, Parameter</td>
<td>1-16</td>
<td>16</td>
<td>Worker internal non-sign-extended data width</td>
</tr>
<tr>
<td>Property</td>
<td>PEAK_MONITOR_p</td>
<td>Bool</td>
<td>-</td>
<td>-</td>
<td>Readable, Parameter</td>
<td>Standard</td>
<td>true</td>
<td>Include a peak detection circuit</td>
</tr>
<tr>
<td>Property</td>
<td>LATENCY_p</td>
<td>UShort</td>
<td>-</td>
<td>-</td>
<td>Readable, Parameter</td>
<td>Standard</td>
<td>1</td>
<td>Number of clock cycles between a valid input and a valid output</td>
</tr>
<tr>
<td>Property</td>
<td>peak</td>
<td>Short</td>
<td>-</td>
<td>-</td>
<td>Volatile</td>
<td>Standard</td>
<td>0</td>
<td>Read-only amplitude which may be useful for gain control</td>
</tr>
</tbody>
</table>

## Component Ports

<table>
<thead>
<tr>
<th>Name</th>
<th>Producer</th>
<th>Protocol</th>
<th>Optional</th>
<th>Advanced</th>
<th>Usage</th>
</tr>
</thead>
<tbody>
<tr>
<td>in</td>
<td>false</td>
<td>iqstream_protocol</td>
<td>false</td>
<td>-</td>
<td>Signed complex samples</td>
</tr>
<tr>
<td>out</td>
<td>true</td>
<td>iqstream_protocol</td>
<td>false</td>
<td>-</td>
<td>Signed complex samples</td>
</tr>
</tbody>
</table>

## Worker Interfaces
dc_offset_filter.hdl

<table>
<thead>
<tr>
<th>Type</th>
<th>Name</th>
<th>DataWidth</th>
<th>Advanced</th>
<th>Usage</th>
</tr>
</thead>
<tbody>
<tr>
<td>StreamInterface</td>
<td>in</td>
<td>32</td>
<td>ZeroLengthMessages=true</td>
<td>Signed complex samples</td>
</tr>
<tr>
<td>StreamInterface</td>
<td>out</td>
<td>32</td>
<td>ZeroLengthMessages=true, InsertEOM=1</td>
<td>Signed complex samples</td>
</tr>
</tbody>
</table>
Control Timing and Signals

The DC Offset Cancellation Filter worker uses the clock from the Control Plane and standard Control Plane signals.
Worker Configuration Parameters

dc_offset_filter.hdl

Table 1: Table of Worker Configurations for worker: dc_offset_filter

Performance and Resource Utilization

dc_offset_filter.hdl

Table 2: Resource Utilization Table for worker "dc_offset_filter"

<table>
<thead>
<tr>
<th>Configuration</th>
<th>OCTP Target</th>
<th>Tool</th>
<th>Version</th>
<th>Device</th>
<th>Registers (Typ)</th>
<th>LUTs (Typ)</th>
<th>Fmax (MHz) (Typ)</th>
<th>Memory/Special Functions</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Stratix IV</td>
<td>Quartus</td>
<td>17.1.0</td>
<td>EP4SGX230KF40C2</td>
<td>465</td>
<td>371</td>
<td>N/A</td>
<td>DSP18</td>
</tr>
<tr>
<td>0</td>
<td>Zynq</td>
<td>Vivado</td>
<td>2017.1</td>
<td>XC7Z020CLG484-1</td>
<td>380</td>
<td>308</td>
<td>N/A</td>
<td>DSP48E1</td>
</tr>
<tr>
<td>0</td>
<td>Zynq</td>
<td>ISE</td>
<td>14.7</td>
<td>XC7Z020CLG484-1</td>
<td>457</td>
<td>355</td>
<td>167.403</td>
<td>DSP48E1</td>
</tr>
<tr>
<td>0</td>
<td>Virtex 6</td>
<td>ISE</td>
<td>14.7</td>
<td>XC7Z020CLG484-1</td>
<td>457</td>
<td>355</td>
<td>165.245</td>
<td>DSP48E1</td>
</tr>
</tbody>
</table>
Test and Verification

Two test cases are implemented to validate the DC Offset Filter component:

1) Normal mode
2) Bypass mode

For both cases, the input file is a waveform with tones at 5 Hz, 13 Hz, and 27 Hz, and adds a DC bias at 0 Hz. The values are scaled to fixed-point signed 16-bit integers, with a maximum amplitude of 22938 to avoid internal overflow.

Time and frequency domain plots may be viewed in Figures 3 and 4 below, respectively, where the time domain plot represents the first 128 complex samples in the file.

For verification of case 1, the output file is first checked that the data is not all zero, and is then checked for the expected length of 32,768 complex samples. Additionally, both the input and output data are translated to the frequency domain, where a FFT is performed, and then power measurements are taken at DC (zero Hz), 5 Hz, 13 Hz, and 27 Hz. The input and output power measurements are compared to validate that the DC bias has been attenuated and that the other tones have not been attenuated. Figures 5 and 6 depict the filtered results of the three tone input. Again, the time domain figure represents the first 128 complex samples in the output time domain file.

![Figure 3: Time Domain Tones with DC bias](image1)

![Figure 4: Frequency Domain Tones with DC bias](image2)

![Figure 5: Time Domain Tones with DC removed](image3)

![Figure 6: Frequency Domain Tones with DC removed](image4)
For case 2, the input data is forwarded to the output port. For verification of this case, the output file is byte-wise compared to the input file.

References
