

Summary - Rectangular to Polar CORDIC

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|-------------------|--|
| Name | rp_cordic |
| Worker Type | Application |
| Version | v1.5 |
| Release Date | 4/2019 |
| Component Library | ocpi.assets.dsp_comps |
| Workers | rp_cordic.hdl |
| Tested Platforms | xsim, isim, modelsim, alst4, ml605, ZedBoard(PL), Matchstiq-Z1(PL) |

Functionality

The Rectangular to Polar CORDIC (Coordinate Rotation Digital Computer) worker implements an FM Discriminator circuit as shown in Figure 1. Complex samples are fed into the CORDIC, which output magnitude and phase values. A $d\phi$ circuit is applied to the phase to calculate real samples.

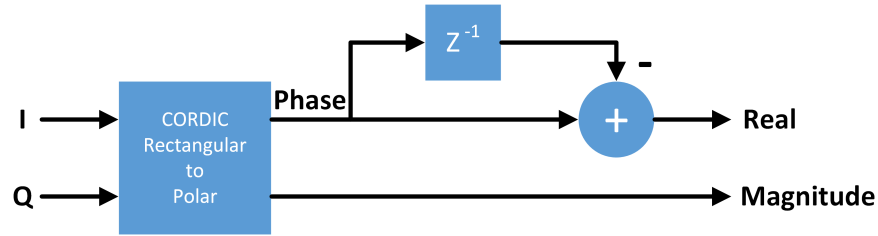


Figure 1: FM Discriminator Block Diagram

Worker Implementation Details

rp_cordic.hdl

The FM Discriminator circuit consists of two sub-circuits: one to calculate the phase and another to calculate the rate of change of the phase. The first circuit uses a CORDIC algorithm to implement the arc-tangent function to calculate the phase of a complex sinusoid. The CORDIC is also used to calculate the magnitude of the complex sinusoid. Equations 1 and 2 represent the equations used to calculate the magnitude and phase, respectively. The magnitude output is exposed as a read-only property of the worker, which could be useful for downstream gain control.

$$magnitude = \sqrt{I^2 + Q^2} \quad (1)$$

$$phase = atan\left(\frac{Q}{I}\right) \quad (2)$$

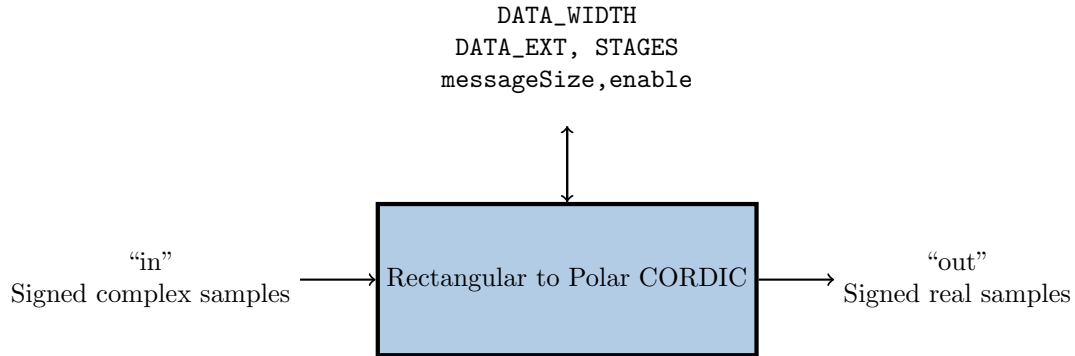
The second circuit simply uses a subtractor to implement a $d\phi$ function, which is a real signed number that is the difference in phase. Equations 3 and 4 show how to calculate $d\phi$.

$$\omega = \frac{d\phi}{dt} = 2\pi f \quad (3)$$

$$d\phi = 2\pi f dt = 2\pi f T_s = \frac{2\pi f}{F_s} = \frac{2\pi f 2^{\frac{DATAWIDTH-1}{\pi}}}{F_s} = \frac{2f * 2^{\frac{DATAWIDTH-1}{\pi}}}{F_s} \quad (4)$$

Block Diagrams

Top level



State Machine

Only one finite-state machine (FSM) is implemented by this worker. The FSM supports Zero-Length Messages.

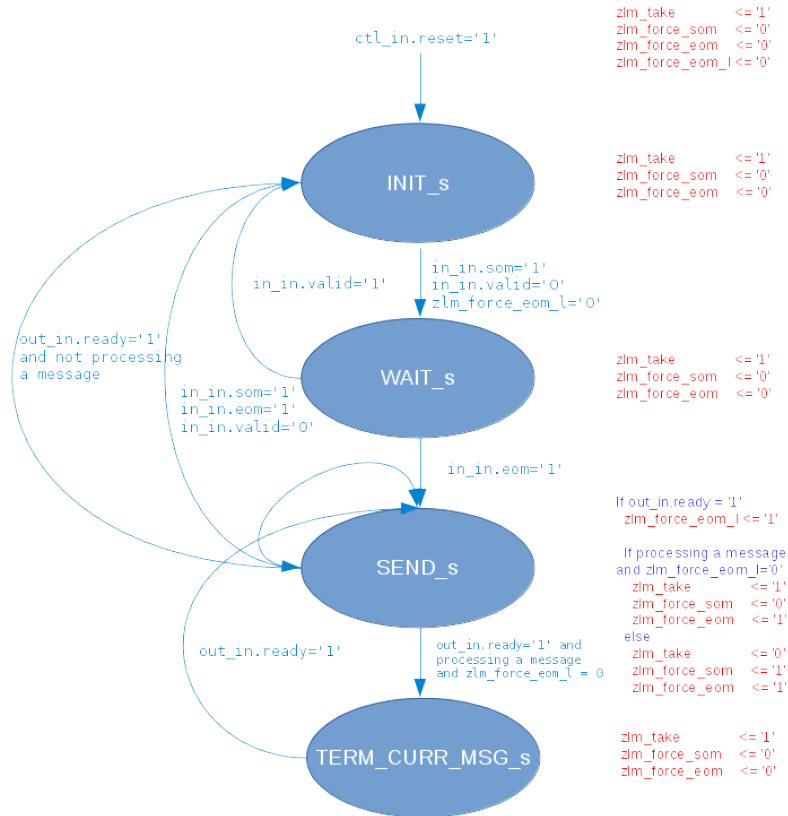


Figure 2: Zero-Length Message FSM

Note: In future releases, this worker will be converted to the HDL version 2 API which will remove the need for this state machine.

Source Dependencies

rp_cordic.hdl

- projects/assets/components/dsp_comps/rp_cordic/rp_cordic.vhd
- projects/assets/hdl/primitives/dsp_prims/dsp_prims_pkg.vhd
 - projects/assets/hdl/primitives/dsp_prims/cordic/src/cordic_rp.vhd
 - projects/assets/hdl/primitives/dsp_prims/cordic/src/cordic.vhd
 - projects/assets/hdl/primitives/dsp_prims/cordic/src/cordic_stage.vhd
- projects/assets/hdl/primitives/misc_prims/misc_prims_pkg.vhd
 - projects/assets/hdl/primitives/misc_prims/round_conv/src/round_conv.vhd

Component Spec Properties

| Name | Type | SequenceLength | ArrayDimensions | Accessibility | Valid Range | Default | Usage |
|-------------|--------|----------------|-----------------|--------------------|-------------|---------|--|
| DATA_WIDTH | UChar | - | - | Readable | - | - | Worker internal non-sign-extended data width |
| DATA_EXT | UChar | - | - | Readable | - | - | # of extension bits |
| STAGES | UChar | - | - | Readable | - | - | Number of CORDIC stages implemented |
| messageSize | UShort | - | - | Writable, Readable | 8192 | 8192 | Number of bytes in output message |
| enable | Bool | - | - | Writable, Readable | Standard | true | Enable/bypass control |

Worker Properties

rp_cordic.hdl

| Type | Name | Type | SequenceLength | ArrayDimensions | Accessibility | Valid Range | Default | Usage |
|--------------|------------|-------|----------------|-----------------|---------------|-------------|---------|--|
| SpecProperty | DATA_WIDTH | - | - | - | Parameter | 8-16 | 16 | Real input and complex output data width |
| SpecProperty | DATA_EXT | - | - | - | Parameter | 6 | 6 | CORDIC requirement: # of extension bits |
| SpecProperty | STAGES | - | - | - | Parameter | 8-16 | 16 | Number of CORDIC stages implemented |
| Property | magnitude | Short | - | - | Volatile | Standard | - | Read-only amplitude which may be useful for gain control |

Component Ports

| Name | Producer | Protocol | Optional | Advanced | Usage |
|------|----------|-------------------|----------|----------|------------------------|
| in | false | iqstream_protocol | false | - | Signed complex samples |
| out | true | rstream_protocol | false | - | Signed real samples |

Worker Interfaces

rp_cordic.hdl

| Type | Name | DataWidth | Advanced | Usage |
|-----------------|------|-----------|-------------------------|------------------------|
| StreamInterface | in | 32 | ZeroLengthMessages=true | Signed complex samples |
| StreamInterface | out | 16 | ZeroLengthMessages=true | Signed real samples |

Control Timing and Signals

The Rectangular to Polar CORDIC worker uses the clock from the Control Plane and standard Control Plane signals. There is a start-up delay for this worker. Once the input is ready and valid and the output is ready, there is a delay of **STAGES+4** before the first sample is taken. After this initial delay, valid output data is given **STAGES+4** clock cycles after input data is taken.

| Latency |
|------------------------------|
| STAGES+3 clock cycles |

Worker Configuration Parameters

rp_cordic.hdl

Table 1: Table of Worker Configurations for worker: rp_cordic

| Configuration | DATA_EXT | DATA_WIDTH | STAGES | ocpi_endian | ocpi_debug |
|---------------|----------|------------|--------|-------------|------------|
| 0 | 6 | 16 | 16 | little | false |

Performance and Resource Utilization

rp_cordic.hdl

Table 2: Resource Utilization Table for worker "rp_cordic"

| Configuration | OCPI Target | Tool | Version | Device | Registers (Typ) | LUTs (Typ) | Fmax (MHz) (Typ) | Memory/Special Functions |
|---------------|-------------|---------|---------|------------------|-----------------|------------|------------------|--------------------------|
| 0 | stratix4 | Quartus | 17.1.0 | EP4SGX230KF40C2 | 1649 | 2623 | N/A | DSP18: 12 |
| 0 | zynq | Vivado | 2017.1 | xc7z020clg484-1 | 1637 | 3613 | N/A | DSP48E1: 3 |
| 0 | zynq_ise | ISE | 14.7 | 7z020clg484-1 | 1584 | 3160 | 145.033 | DSP48E1: 6 |
| 0 | virtex6 | ISE | 14.7 | 6vlx240tff1156-1 | 1584 | 3160 | 145.455 | DSP48E1: 6 |

Test and Verification

One test case is implemented to validate the Rectangular to Polar CORDIC component:

1) Normal mode

The input file is a waveform with a single tone at 27 Hz sampled at 10 kHz. The complex waveform is then scaled to fixed-point signed 16-bit integers, using a maximal amplitude of 32,767. Time and frequency domain plots may be viewed in Figures 3 and 4 below, respectively.

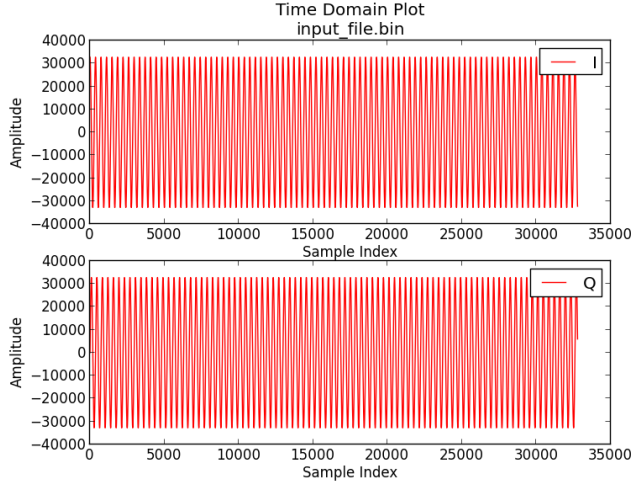


Figure 3: Time Domain Complex Tone

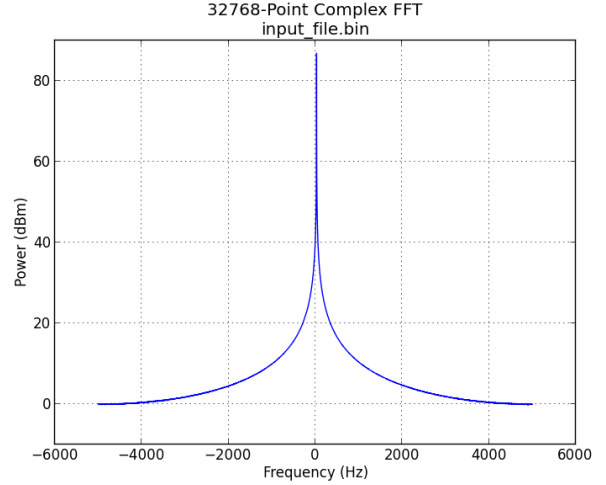


Figure 4: Frequency Domain Complex Tone

The output file is first checked that the data is not all zero and is then checked for the expected length. Once these quick checks are made, the complex input data is transformed into expected magnitude and phase arrays using Equations 1 and 2. The expected phase array then implements the FM discriminator subtractor to create an array of the expected phase difference. These two expected value arrays are compared sample-by-sample with the measured phase output array from the UUT and the single value magnitude property from the UUT. Error checks are then calculated for the average peak error, the magnitude peak error, and the phase peak error. Should any of these three error values be more than one (the difference between each expected and measured value is allowed to be no greater than one) the overall test fails. Figure 5 depicts the conversion results of the single tone input, which shows no more than a ± 1 deviation from the expected result. Equation 4 is used to form Equation 5, which validates the result shown in Figure 5.

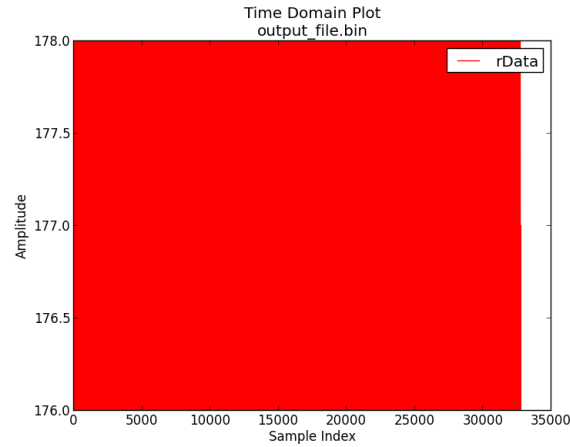


Figure 5: Time Domain Real Data

$$d\phi = \frac{2f * 2^{DATAWIDTH-1}}{F_s} = \frac{2 * 27 * 32,768}{10,000} = 176.9472 \quad (5)$$