Summary - MFSK Mapper

Name	mfsk_mapper
Worker Type	Application
Version	v1.5
Release Date	4/2019
Component Library	ocpi.assets.comms_comps
Workers	mfsk_mapper.hdl mfsk_mapper.rcc
Tested Platforms	xsim, isim, modelsim, Matchstiq-Z1(PL), zed, alst4, ml605, e3xx, xilinx13_3, xilinx13_3

Functionality

The MFSK Mapper component translates bits or groups of bits to Q0.15 signed real FSK symbol values.

The number of FSK symbols is set with the `M_p` parameter, and the number of bits per FSK symbol is related by 1.

$$bits\_per\_symbol = log2(M\_p) \tag{1}$$

The MFSK Mapper component parses the bits on its input in bits per symbol sized pieces. The parsing begins on the MSB and ends on the LSB.

The possible FSK symbol values that can appear on the output of the component is set with the property `symbols`. `symbols` is an array property with Q0.15 values with size `M_p`. The FSK symbol value produced on the output will be the value of the symbols property at the index equal to value of the bits being parsed.

For example, if `M_p` was set to 4, the number of bits per symbol is equal to 2 and the symbols property is an array with 4 values indexed from 0 to `M_p`. If the bit sequence 00011011 appeared on the input, it would be interpreted as 4 symbols: 00,01,10,11. The output of the component would be equal to symbols[0], symbols[1], symbols[2], and symbols[3].

Worker Implementation Details

mfsk_mapper.hdl

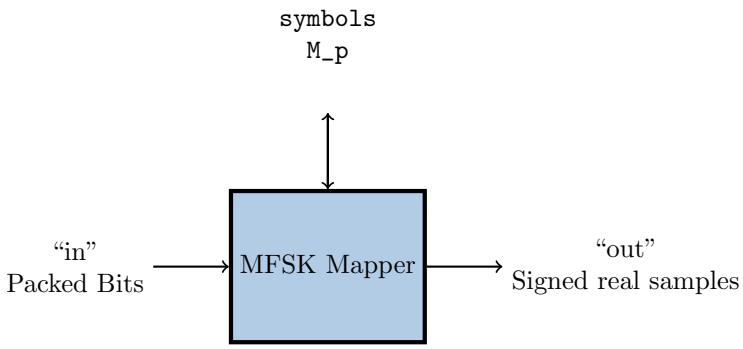
The message size for the output is equal to DIN_WIDTH_p divided by the number of bits per symbol multiplied by 2.

mfsk_mapper.rcc

The message size for the output is equal to the input message size in bits divided by the number of bits per symbol multiplied by 2.

Block Diagrams

Top level



Source Dependencies

mfsk_mapper.hdl

- ocpiassets/components/comms_comps/mfsk_mapper.hdl/mfsk_mapper.vhd

Component Spec Properties

Name	Type	SequenceLength	ArrayDimensions	Accessibility	Valid Range	Default	Usage
M_p	UChar	-	-	Readable, Parameter	2,4	2	Number of FSK levels
symbols	Short	-	M_p	Readable, Writable	Standard	-	FSK symbol values

Worker Properties

mfsk_mapper.hdl

Type	Name	Type	SequenceLength	ArrayDimensions	Accessibility	Valid Range	Default	Usage
Property	DIN_WIDTH_p	Ulong	-	-	Readable, Parameter	16	16	Input port data width

Component Ports

Name	Producer	Protocol	Optional	Advanced	Usage
in	false	-	false	-	Packed bits
out	true	rstream_protocol	false	ZeroLengthMessages=true	Q0.15 signed real samples

Worker Interfaces

mfsk_mapper.hdl

Type	Name	DataWidth	Advanced	Usage
StreamInterface	in	DIN_WIDTH_p	-	Packed bits
StreamInterface	out	16	-	Q0.15 signed real samples

Control Timing and Signals

The MFSK Mapper HDL worker uses the clock from the Control Plane and standard Control Plane signals.

Worker Configuration Parameters

mfsk_mapper.hdl

Table 1: Table of Worker Configurations for worker: mfsk_mapper

Configuration	ocpi_debug	ocpi_endian	DIN_WIDTH_p	M_p
0	false	little	16	2
1	false	little	16	4

Performance and Resource Utilization

mfsk_mapper.hdl

Table 2: Resource Utilization Table for worker "mfsk_mapper"

Configuration	OCPI Target	Tool	Version	Device	Registers (Typ)	LUTs (Typ)	Fmax (MHz) (Typ)	Memory/Special Functions
0	stratix4	Quartus	17.1.0	EP4SGX230KF40C2	224	240	N/A	N/A
0	zynq	Vivado	2017.1	xc7z020clg484-1	221	250	N/A	N/A
0	zynq_ise	ISE	14.7	7z020clg484-1	217	621	264.201	N/A
0	virtex6	ISE	14.7	6vlx240tff1156-1	217	634	247.831	N/A
1	stratix4	Quartus	17.1.0	EP4SGX230KF40C2	255	278	N/A	N/A
1	zynq	Vivado	2017.1	xc7z020clg484-1	252	319	N/A	N/A
1	zynq_ise	ISE	14.7	7z020clg484-1	248	579	264.201	N/A
1	virtex6	ISE	14.7	6vlx240tff1156-1	248	592	247.831	N/A

Test and Verification

The input file consists of packed bits with a series of ramps from 0 to the number of FSK levels minus 1. The

The expected output waveform is a matching series of ramps of 16 bit values from 0 to the number of FSK levels minus 1. For verification, the values in the ramp are verified to match the input.