Zipper Deprecation Notice:

Beginning with OpenCPI Version 1.5, support for Lime Microsystems' Zipper card is now deprecated.

Summary - Lime DAC

Name	lime_dac
Worker Type	Device
Version	v1.5
Release Date	4/2019
Component Library	ocpi.assets.devices
Workers	lime_dac.hdl
Tested Platforms	• Epiq Solutions Matchstiq-Z1 • Digilent Zedboard/Zipper • x86/Xilinx ML605/Zipper (FMC-LPC/FMC-HPC) • x86/Altera ALST4/Zipper (HSMC A/B)

Functionality

The Lime DAC device worker converts the OpenCPI WSI interface into the Lime LMS6002Dr2 Transceiver DAC interface. The data enters the worker in the control clock domain and is converted to the sample clock domain (DAC_CLK).

Worker Implementation Details

lime_dac.hdl

The clock domain crossing (CDC) from the OpenCPI control clock to the sample clock is performed using a two-clocked synchronizing FIFO. The WSI interface can be seen in Figure 1. The incoming 32 bit data contains one complex sample, with the lower 16 bits containing I and the upper 16 bits containing Q. Before it is loaded into the CDC FIFO, the 32 bit sample is reduced to 24 bits by taking the top 11 bits and rounding the 12th bit for both I and Q. The FIFO has a data width of 24 bits and depth of 64. Data is loaded into the FIFO when the upstream worker is ready and unloaded using TX_IQ_SEL. In the event that a sample cannot be unloaded from the FIFO, the `underrun` property is set and remains set until it is cleared. The FIFO output signals are then translated into the DAC interface.

Figure 2 shows the Lime DAC Interface in the sample clock domain. There are 14 output signals in the interface: DAC_CLK(1), TX_IQ_SEL(1), and TXD(12). One data sample (I and Q) is clocked in every two DAC_CLK cycles with TX_IQ_SEL serving as the qualifier for the I sample. The data width for the DAC is 12 bits and the data format is two's complement.

DAC_CLK can originate from one of two sources based on the value of the parameters. The table below describes the valid settings.

USE_CLK_IN_p	USE_CTL_CLK_p	DAC_CLK
True	X	TX_CLK_IN
False	True	ctl_in.clk

TX_CLK can be driven by this worker by setting the DRIVE_CLK_p parameter or it can be driven from another source external to the worker.

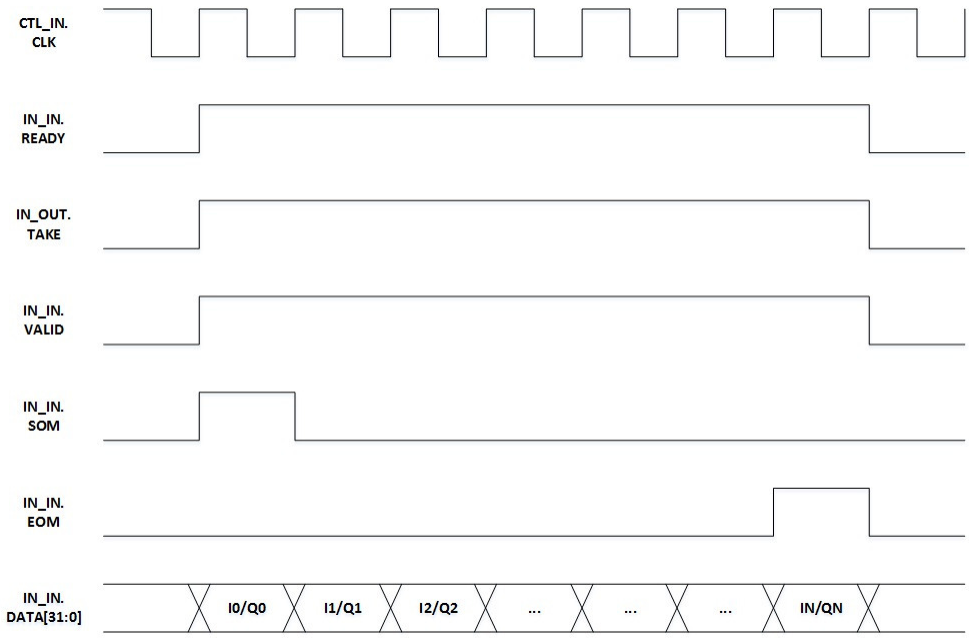


Figure 1: WSI Interface: Control Clock Domain

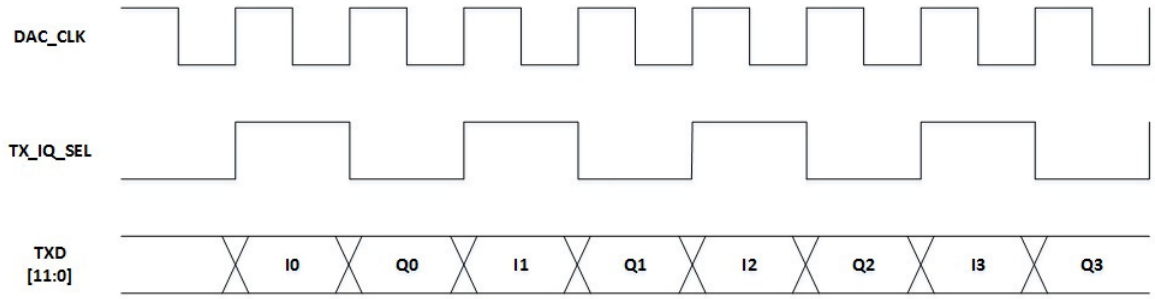


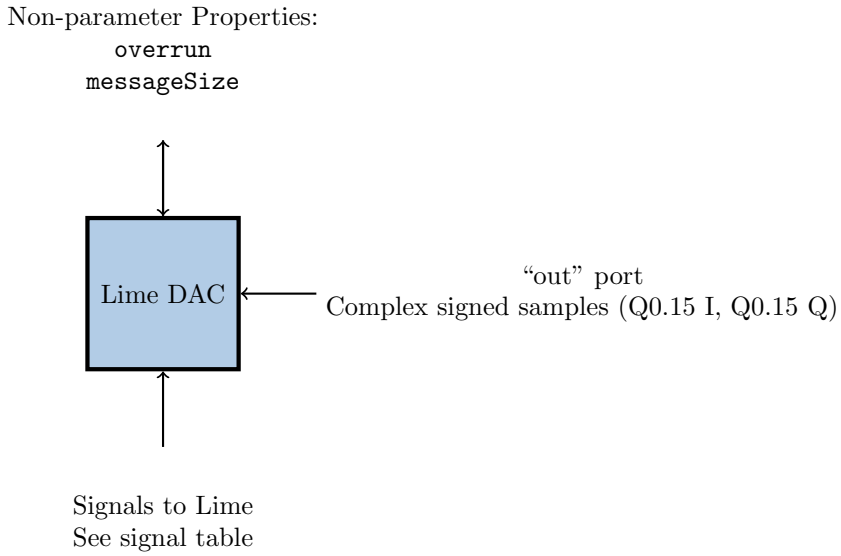
Figure 2: Lime DAC Interface: Sample Clock Domain

Theory

The main purpose of this worker is to perform a CDC for a data bus. The decision was made to implement the CDC using a two-clocked FIFO in an effort to target resources native the FPGA.

Block Diagrams

Top level



Source Dependencies

lime_dac.hdl

- assets/hdl/devices/lime_dac.hdl/lime_dac.vhd
- core/hdl/primitives/util/dac_fifo.vhd
  - Performs the clock domain crossing between the control clock and sample clock domains
  - assets/hdl/devices/lime_adc.hdl/sync_status.vhd
    - Generates the *underrun* event when the DAC tries to unload a sample and the DAC FIFO is empty
  - core/hdl/primitives/bsv/imports/SyncFIFO.v
    - Two-clocked CDC FIFO

Component Spec Properties

Name	Type	SequenceLength	ArrayDimensions	Accessibility	Valid Range	Default	Usage
underrun	Bool	-	-	Volatile, Writable	Standard	-	Flag set when DAC tries to send a sample and the DAC FIFO is empty. Once high, this flag is not cleared (i.e. set low) until the property is written to again (the flag clears regardless of write value, i.e. writing true or false both result in a value of false).

Worker Properties

lime_dac.hdl

Type	Name	Type	SequenceLength	ArrayDimensions	Accessibility	Valid Range	Default	Usage
Property	fifo_depth	ULong	-	-	Parameter	Standard	64	Depth in number of samples of the control-to-DAC clock domain crossing FIFO.
Property	IDATA_WIDTH_p	UShort	-	-	Parameter	Standard	32	
Property	min_num_cp_clks_per_txen_events	UShort	-	-	Initial, Readable	Standard	938	After every ZLM received on the event_in port, backpressure will be held on that port for one less than the number of control plane clock cycles specified by this property. This is done in order to ensure tx events are properly synchronized to the DAC clock without losing any events. Minimum required value is ceil(1.5 * control plane clock rate / DAC clock rate [use lowest expected DAC clock rate for your scenario]).
Property	other_present	Bool	-	-	Readable	-	-	Not implemented. Flag to indicated presence of ADC worker
Property	DRIVE_CLK_p	Bool	-	-	Parameter	Standard	1	Drive the clock sent to Lime (TX_CLK). Some platforms do not connect TX_CLK to the FPGA, making this parameter false
Property	USE_CLK_IN_p	Bool	-	-	Parameter	Standard	0	Use copy of clock sent to Lime (TX_CLK) as DAC_CLK.
Property	USE_CTL_CLK_p	Bool	-	-	Parameter	Standard	1	Use control clock as DAC_CLK. This is primarily for testing the component.
Property	divisor	-	-	-	Writable	-	-	Not implemented. Divider for DAC clock. This is primarily for testing the component.
SpecProperty	underrun	-	-	-	-	-	0	This property is set when the DAC tries to unload a sample and the DAC FIFO is empty.

Component Ports

Name	Producer	Protocol	Optional	Advanced	Usage
in	False	iqstream_protocol	False	-	Complex signed samples (Q0.15 I, Q0.15 Q).
event_in	False	tx_event-prot	False	-	TX on/off events.

Worker Interfaces

lime_dac.hdl

Type	Name	DataWidth	Optional	Advanced	Usage
StreamInterface	in	32	False	-	Complex signed samples (Q0.15 I, Q0.15 Q). This port ingests data and forces backpressure. Because both a “pulling” pressure from the DAC clock and potentially limited “pushing pressure” from this port exists, it is possible for a value to be clocked to the DAC while no new value was yet seen at the in port. This event is monitored via the `underrun` property.
StreamInterface	event_in	-	True	-	TX on/off events.
DevSignal	dev_txen	-		-	txen-out-signals - Signal for controlling the Tx_EN pin of the Lime transceiver device
DevSignal	dev_tx_event	-		-	lime-tx-event-signals - Bus interface signals to the lime_spi.hdl worker, which subsequently controls the Tx_EN register bit value.

Signals

Name	Type	Width	Description
TX_CLK	Output	1	Clock input to Lime
TX_IQ_SEL	Output	1	IQ Select to Lime
TXD	Output	12	Lime DAC data bus. IQ interleaved
TX_CLK_IN	Input	1	Copy of TX_CLK sent to FPGA

Control Timing and Signals

The Lime DAC device worker uses the clock from the Control Plane and Control Plane signals.

The latency through the worker from the input port to the DAC pins is 1 control clock cycle and 2 sample clock cycles. The data is loaded from the input port into the FIFO in one control clock cycle and unloaded to the DAC pins every other sample clock cycle (when TX_IQ_SEL is high).

Worker Configuration Parameters

lime_dac.hdl

Table 1: Table of Worker Configurations for worker: lime_dac

Configuration	USE_CTL_CLK_p	DRIVE_CLK_p	ocpi_endian	USE_CLK_IN_p	ocpi_debug
0	0	1	little	1	false

Performance and Resource Utilization

lime_dac.hdl

Table 2: Resource Utilization Table for worker "lime_dac"

Configuration	OCPI Target	Tool	Version	Device	Registers (Typ)	LUTs (Typ)	Fmax (MHz) (Typ)	Memory/Special Functions
0	stratix4	Quartus	17.1.0	N/A	305	318	N/A	Block Memory Bits: 1536
0	zynq	Vivado	2017.1	xc7z020clg400-3	308	329	N/A	BUFGCTRL: 1 BUFG: 1 RAMB18E1: 1
0	zynq_ise	ISE	14.7	7z010clg400-3	324	554	429.465	BUFGCTRL: 1 BUFG: 1 RAM64M: 8
0	virtex6	ISE	14.7	6vcx75tff484-2	324	552	341.28	BUFGCTRL: 1 BUFG: 1 RAM64M: 8

Test and Verification

To be detailed in a future release.

References

1) LMS6002D Datasheet, www.limemicro.com